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cost, and associated chip real estate corresponding to prior art methods for achieving the same result.

Brief Description of the Drawing

The invention will be better understood from a reading of the following detailed description taken in conjunction with the drawing in which like reference designators are used to designate like elements, and in which:

- FIG. 1 is a circuit model diagram of a conventional output buffer of an integrated circuit;
- FIG. 2A is a top view of a conventional circuit board with integrated circuit devices thereon;
 - FIG. 2B is a cross-sectional view of the circuit board of FIG. 2A;
 - FIG. 2C is a cross-sectional view of the integrated circuit of FIG. 2A;
- FIG. 3 is an operational flowchart of a method for controlling the slew rate of integrated circuit signals in accordance with the invention;
- FIG. 4A is a plan view of an example of a die pad layout pattern for the die of FIG. 2A-2C:
- FIG. 4B is a plan view of the die of FIG. 4A illustrating an output pad block :
- FIG. 4C is an exploded view of a portion of the die of FIG. 4B illustrating the mapping of a first output driver cell to a die pad;
- FIG. 4¢ is an exploded view of the portion of the die of FIG. 4B illustrating the mapping of a second output driver cell to a die pad;
- FIG. 4E is a completed output-driver-to-pad mapping for the output driver block of FIG. 4B;
- FIG. 5A is a side cross-sectional view of an integrated circuit device illustrating an example output driver-to-transmission line interconnect path; and
- FIG. 5B is a top plan view of the integrated circuit device illustrating the example output driver-to-transmission line interconnect path of FIG. 5B.

Detailed Description

A novel technique for controlling the slew rate of output signals of integrated circuits using signal redistribution metal is described in detail

Agilent Docket No. 10011019-1